In the Claims:

What is claimed is:

1. (currently amended) A device for electrostatic discharge input protection comprising:

a transistor with gate, source, drain and substrate terminals;

an input signal terminal coupled to said source terminal of said transistor;

a reference point coupled to said gate and substrate terminals of said transistor;

and

an ~~a~~ output signal terminal coupled to said drain terminal of said transistor;

where under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and the leakage current of said transistor is reduced to a sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and reduces its threshold voltage.

2. (original) The device of claim 1 wherein said reference point comprises the ground for a specific electrostatic discharge application.

3. (original) The device of claim 1 wherein said reference point is 0 volts.

4. (currently amended) The device of claim 1 wherein said reference point comprises ~~Vss~~ the lower potential supply terminal Vss.

5. (original) The device of claim 1 wherein said source voltage is a few 100mV.

6. (original) The device of claim 5 wherein said leakage current is approximately 10^{-14} A/um.

7. (original) The device of claim 1 wherein said transistor is an NMOS transistor.

8. (original) The device of claim 1 wherein said transistor is a PMOS transistor.

9. (currently amended) A low leakage Electrostatic Discharge (ESD) protection scheme comprising:

a plurality of low operating voltage devices, each device having at least one device input for receiving an input signal;

a plurality of input terminals for coupling an input signal to a device via a corresponding device input;

a plurality of transistors with gate, substrate, source and drain terminals,

each transistor providing an alternate pathway via a source terminal for signals from said plurality of input terminals; and

a reference coupled to corresponding gate and substrate terminals of said plurality of input protection transistors; and

a source voltage driving both said source terminals of said input protection transistors and said inputs of said low operating voltage devices;

wherein under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and ESD protection is achieved by coupling the source terminals of said plurality of transistors to said plurality of input terminals thereby limiting the leakage current of each of said transistors to a sub-threshold level even as said source voltage increases.

10. (original) The protection scheme of claim 9 wherein said plurality of low operating voltage devices are CMOS.

11. (original) The protection scheme of claim 9 wherein said reference point comprises a ground reference.

12. (original) The protection scheme of claim 9 wherein said reference point is 0 volts.

13. (currently amended) The protection scheme of claim 9 wherein said reference point comprises ~~Vss~~ the lower potential supply terminal Vss for said low voltage operating devices and said plurality of transistors.

14. (original) The protection scheme of claim 9 wherein said source voltage is limited to a few 100mV.

15. (original) The protection scheme of claim 14 wherein the resulting leakage current from said source voltage is approximately 10^{-14} A/um.

16. (original) The protection scheme of claim 9 wherein said plurality of transistors are NMOS type.

17. (original) The protection scheme of claim 9 wherein said plurality of transistors are PMOS type.

18. (original) A low voltage Integrated Circuit (IC) with on-board ESD input protection comprising:

a plurality of low operating voltage devices,

at least one reference point, one supply voltage point and a plurality of input terminals coupled to said devices;

a plurality of input paths for coupling input signals to said devices via said input terminals; and

a plurality of input protection transistors with gate, substrate, source, and drain terminals arranged between said input paths and said devices, each source terminal coupled to a corresponding input path, each gate and substrate terminal coupled to a reference point;

wherein a leakage current of said input protection transistors is controlled to a sub-threshold level over a range of voltages applied to each source terminal of said input protection transistors.

19. (original) The IC of claim 18 wherein said plurality of input protection transistors are NMOS type.

20. (original) The IC of claim 18 wherein said plurality of input protection transistors are PMOS type.

21. (original) The IC of claim 18 wherein said devices, terminals, input paths, and input protection transistors are contained on a single semiconductor chip.

22. (original) The IC of claim 18 wherein said reference point is a ground reference point associated with said devices.

23. (original) The IC of claim 18 wherein said reference point is a 0 volt point associated with said devices.

24. (currently amended) The IC of claim 18 wherein said reference point is tied to said ~~Vss~~ lower potential supply terminal Vss.